

Docket No.: 42390.P7876X

### **REMARKS**

#### **Cross-Reference to Related Application**

The Examiner pointed out the procedure for claiming priority to an earlier application under 35 U.S.C. § 120. Thank you. The Applicant has amended the specification herein to properly present the claim for priority to Application No. 09/475,614 filed December 30, 1999, pending. It should be noted that the Applicant presented the claim for priority in the Declaration, the priority claim appeared on the Filing Receipt of the present application, and the present application was filed on July 27, 2000.

#### **Objections to the Drawings**

The Examiner objected to the drawings because the legends or not legible. The Applicant is submitting herewith corrected drawings for FIG. 1 through FIG. 11. No new drawings are being submitted for FIG. 12 through FIG. 14 since those drawings are legible and, although the Examiner did not specify which drawings he thought were illegible, it appeared that the Examiner was referring to FIG. 1 through FIG. 11.

The Examiner stated that there is no description of Figure 2 in the specification. The specification does in fact include a description of Figure 2. A typographical error appears on page 6, at line 10. The sentence "Referring to FIG. 3" should read "Referring to FIG. 2". The specification has been amended herein to correct this typographical error. Thus the description of Figure 2 appears at least from page 6, line 10 to page 7, line 21.

The Examiner has requested that the Applicant identify the network, the network data, the first and the second threads, the network processor and its components for scheduling threads in the drawings and the corresponding description in the specification.

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Such items whose identification the Examiner requested appear throughout the drawings and are described throughout the specification. Please note the following:

**Network**

The word “network” appears for example in the preamble of claim 1 but is not recited as an element of the Applicant’s claims but merely to set forth the intended use of the network processor (MPEP § 2111.02). See the description of “network data” below.

**Network Data**

“Network data” is packet data received for example from devices 30 and 31 as shown in FIG. 1. The invention operates on network data such as packet data. For example, please refer to the specification on page 5, lines 21-25 through page 6 lines 1-2:

The processor 12 functioning as a network process could receive units of packet data from the devices 30, 31 and process those units of packet data in a parallel manner, as will be described. The unit of packet data could include an entire network packet (e.g., Ethernet packet) or a portion of such a packet.

So, as known to those of ordinary skill in the art, a network processor is a processor that processes network data, for example packet data, transmitted via a network, such as Ethernet, although the scope of the invention is not limited in this respect. See also FIG. 12 and its description on page 23, lines 12-25.

**Network Processor**

A network processor is shown for example in FIG. 1 as item 12. The Examiner’s attention is also kindly directed to the specification on page 5 at lines 23-25”

The processor 12 functioning as a network processor could receive units of packet data from the devices 30, 31 and process those units of packet data in a parallel manner, as will be described.

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So a reading of the specification reveals that the network processor is processor 12 in at least one embodiment of the invention, although the scope of the invention is not limited in this respect.

#### **First and Second Threads**

The specification describes various threads throughout. For example, the processor 12 is described as a "**multi-threaded** processor 12" such as on page 5 at line 13. Multiple threads are shown, for example, in FIG. 3 in thread task assignment box 90 in which a "**plurality of threads** are configured as **receive processing threads 96** and **transmit processing (or "fill") threads 98**" such as described on page 7 line 26 through page 8 line 4. In one embodiment of the invention, any one of more of the plurality of these threads may be a first thread or a second thread, although the scope of the invention is not limited in this respect. See also FIG. 12 and its description on page 23, lines 12-25.

#### **Components for Scheduling**

Components for scheduling may include for example a receive scheduler thread 92 as shown in FIG. 3 and described for example in the specification on page 8 at line 5, "The **receive scheduler thread 92** assigns packets to receive processing threads 96." Thus, it appears that the Examiner's identification request has been satisfied.

#### **35 U.S.C. §112 Rejection**

The Examiner rejected claims 3-6 under 35 U.S.C. § 112, second paragraph, as being indefinite failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

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Regarding claim 3, the Examiner stated, "It is not clear why the second and not the first thread retrieves the state information after interrupt." The Applicant respectfully traverses the rejection. The Examiner's attention is kindly directed, for example, to the specification at page 23, lines 13-25:

In Figure 12, the receive scheduler initiates three receive requests one after another (301). Each receive request initiates a bus transfer that wakes up an available thread (302). Thread X 303 is the first thread to wake up. It retrieves control information and saves state, as will be described in more detail later, and then continues to process network data. Passing state information early on in the thread processing allows the network processor to maintain a high data rate since the threads processing allows the network processor to maintain a high data rate since the threads can continue to process their packets at their own slower pace.

Thread Y 304 wakes up from the second bus transfer. Similar to thread X, thread Y retrieves control information, saves state, then processes its network data. Thread Z 305 behaves similarly. If threads X, Y, and Z are in different microengines, then each thread may proceed without context switching relative to each other.

So it is clear from at least this disclosure in the specification the scope of claim 3.

Regarding claim 6, the Examiner stated, without any further reasoning or explanation:

Scope of claim 6 is not clear.

The Applicant hereby respectfully traverses the rejection. The Examiner's attention is kindly directed to MPEP 2173.04:

#### **2173.04 Breadth is Not Indefiniteness**

Breadth of a claim is not to be equated with indefiniteness. *In re Miller*, 441 F.2d 689, 169 USPQ 597 (CCPA 1971). If the scope of the subject matter embraced by the claims is clear, and if applicants have not

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otherwise indicated that they intend the invention to be a scope different from that defined in the claims, then the claims comply with 35 U.S.C. 112, second paragraph.

Thus, since the Examiner has not set forth any reasoning why the scope of claim 6 is not clear, the Examiner has not met the burden of establishing an indefiniteness rejection under § 112. Therefore, the rejection should be withdrawn.

### 35 U.S.C. §103 Rejection

#### *Mohamed (6,366,998)*

The Examiner rejected claims 1 and 7- 14 under 35 U.S.C. § 103(a) as being unpatentable over Mohamed (US 6,366,998). Contrary to the Examiner's assertion, the patent to Mohamed does not disclose "*scheduling a second thread to process a second incoming block of data prior to the first thread completing*" as claimed in independent claim and its dependent claims. In fact, the Examiner did not even address or explain where in the patent to Mohamed that the limitation of *prior to the first thread completing* is suggested or taught. The Examiner is kindly reminded that, in order to satisfy the burden of establishing a *prima facie* obviousness rejection,

the prior art reference (or references when combined) must teach or suggest all of the claim limitations. MPEP §§ 2142, 2143.

Thus, since the Examiner did not establish a *prima facie* obviousness rejection, the rejection should be withdrawn.

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**Mohamed (6,366,998) v. Anderson et al. (3,736,566)**

The Examiner rejected claims 2-6 and 15-17 under 35 U.S.C. § 103(a) as being unpatentable over Mohamed (US 6,366,998) in view of Anderson et al. (US 3,736,566).

As described with respect to claim 1, above, the Examiner did not address or explain how Mohamed teaches, discloses or suggests *"scheduling a second thread to process a second incoming block of data prior to the first thread completing"*, nor has the Examiner shown the same with respect to the Anderson patent. Therefore the rejection of claims depending from claim 1 should be withdrawn.

Regarding claims 15-17, contrary to the Examiner's assertion, neither the patent to Mohamed nor the patent to Anderson teaches or discloses that *"there is no time sharing between the first thread and the second thread"* as claimed in independent claim 15 and its dependent claims. In fact, the Examiner's rejection is completely silent on the concept of *time sharing*. As a result, the Examiner has not shown that the prior art teaches or suggests all of the limitations of the Applicant's claims such that the Examiner has not met the burden of establishing a prima facie obviousness rejection as set forth in MPEP §§ 2142, 2143, so the rejection should be withdrawn.

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### Conclusion

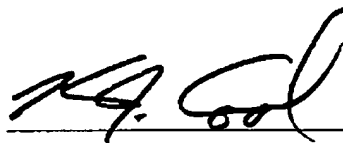
In light of the foregoing, reconsideration and allowance of the claims is hereby earnestly requested.

### Invitation for a Telephone Interview

The Examiner is invited to call the undersigned attorney, Kenneth J. Cool, at (408) 850-1229 if there remains any issue with allowance.

Respectfully submitted,  
INTEL CORPORATION

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